Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov/Dec – 2018**

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| **Code :** | **14EC2026** | **Duration :** | **3hrs** |
| **Sub. Name :** | **ADVANCED MICROPROCESSOR ARCHITECTURE** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Examine the operation of the following sequence of instructions in terms of addressing modes.   1. Move (R5)+, R0 2. Add (R5)+, R0 3. Move R0, (R5) 4. Move 16(R5),R3 5. Add R5,#40 | CO1 | 6 |
| b. | With a neat block diagram narrate the components of a computer system. | CO1 | 7 |
| c. | State and prove Amdahl’s law. | CO1 | 7 |
| (OR) | | | | |
| 2. | a. | Assess the Operations and operands for media and signal processing in ISA. | CO1 | 7 |
| b. | List out the difficulties in implementing pipelines in a processor design. | CO1 | 7 |
| c. | Appraise the performance of a microprocessor using technology trends and cost price trends. | CO1 | 6 |
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| 3. | a. | Discuss the best classification of parallel system- Flynn’s or Handeler’s. Deliberate the llimitations, if any. | CO2 | 7 |
| b. | Describe various types of instruction level parallelism. | CO2 | 7 |
| c. | Distinguish between multiprocessors and multicomputers based on their structures and resourse sharing. | CO2 | 6 |
| (OR) | | | | |
| 4. | a. | Defend how the multicycle operations are handled by extended MIPS pipeline. | CO2 | 10 |
| b. | Relate the role of inclusion, coherence and locality properties in memory hierarchy technology. | CO2 | 10 |
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| 5. | a. | Categorise and examine the types of multiprocessors using necessary diagrams. | CO2 | 12 |
| b. | Express the operation of message passing algorithm in multicomputers. | CO2 | 8 |
| (OR) | | | | |
| 6. | a. | “The mototrola MC68040 CISC microprocessor has the characteristics of RISC processor”Justify the statement using necessary diagrams. | CO3 | 10 |
| b. | Elaborate the concept of advanced processor technology | CO3 | 6 |
| c. | Define the term “under utilization” of pipelines | CO3 | 4 |
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| 7. | a. | What is branch prediction? Explain the role of it in super scalar processor. | CO3 | 10 |
| b. | Brief the three functional units of IBM RS/6000 advanced processor architecture. | CO3 | 10 |
| (OR) | | | | |
| 8. | a. | Use the pipeline structure to illustrate the function of a VLIW advanced processor of degree 3. | CO3 | 12 |
| b. | Compare superscalar processor and VLIW processor | CO3 | 5 |
| c. | Mention the applications of VLIW processor. | CO3 | 3 |
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|  | | **Compulsory**: |  |  |
| 9. | a. | Assess the role of vector instruction in reducing the vector processor computation. | CO3 | 8 |
| b. | Compare the pipelined execution with its scalar counter part in vector processors. | CO3 | 8 |
| c. | Briefly characterize symbolic processor | CO3 | 4 |